***AEC* *LAB REPORT – 5***

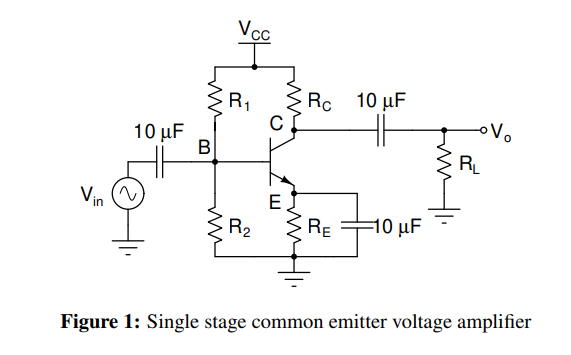
***BJT Amplifier***

***NAME:*** *Khyathi Sri Basireddy*

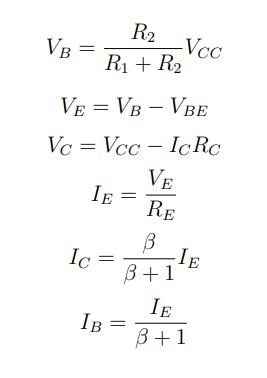
***ROLL NO****: 2023102065*

***TABLE NO: 9***

*The circuit we will be analyzing is a Common Emitter (CE) voltage amplifier.*

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***Equations that can be used are listed below:***

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***1. DC Analysis***

**Given parameters:**  
R1 = 5.6K Ohm

R2 = 1K Ohm

RL = 1K Ohm

VCC = 12 Volt

IC = 1.5 mA

VBE = 0.7 V

β = 150

Gain = |AV| = 5

Gain = gm. Ro

gm = IC / VT

When we do a DC analysis of a circuit, we “***Open”*** all the capacitors since they don’t allow the AC signals to pass.

The simplified circuit looks like the following after opening the capacitors.

***Required to find***: RC and RE

**Calculations:**

• IB = IC / β

= 1.51 X 10-3 / 150

= 10 uA

VB = (R2 / R1 + R2). VCC

= 12/6.6

= 1.818. V

VE = VB – VBE

= 1.818 – 0.7

= 1.118 V

• IE = IB + IC

= 10 uA + 1.5 mA

= 1.51 mA

RE = VE / IE

= 1.118 / 1.51 x 10-3

**RE= 740.3 ohm**

To find the gain, consider the AC analysis of the circuit

Gain = gm (RL || RC)

5 = (IC / VT) (RL || RC)

RL || RC = 5 x 26m/1.5m

RL || RC = 86.667 ohm

Substitute the value of RL

**RC = 94.8 ohm**

***2. Transient response and total harmonic distortion (THD)***

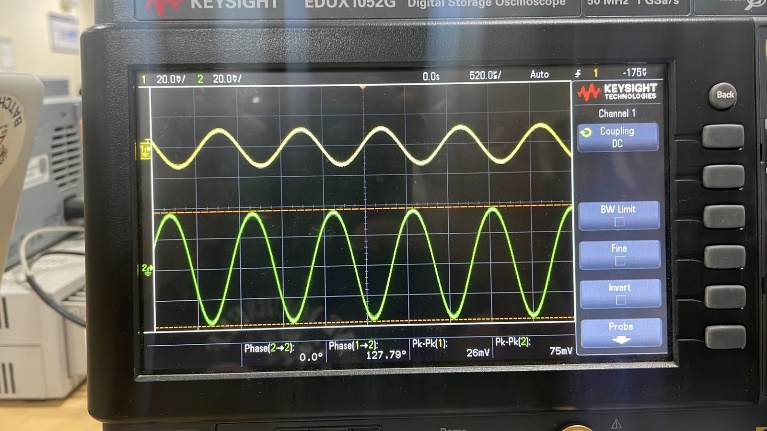
**Given,**

Input 🡪 sine wave

Vpp = 25 mV

F = 1k Hz

RL = 1k ohm



Vout = 75 mV

Gain = Vout / Vin

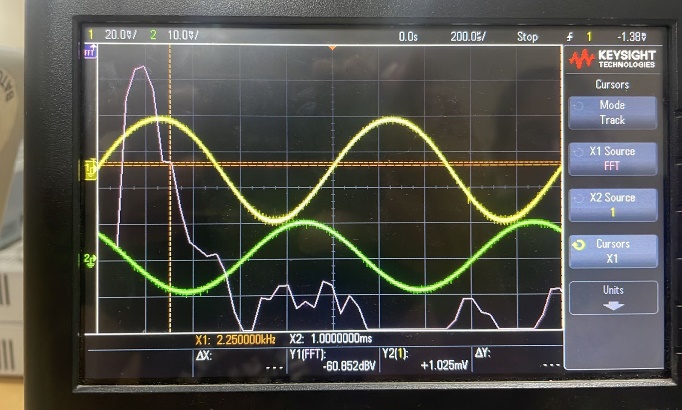
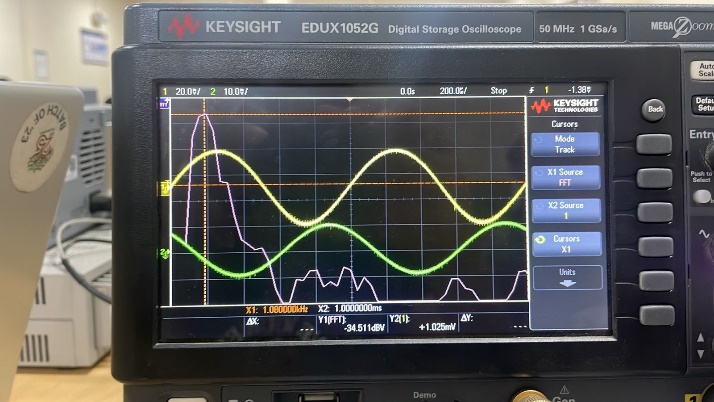
= 75m/25m

= 3

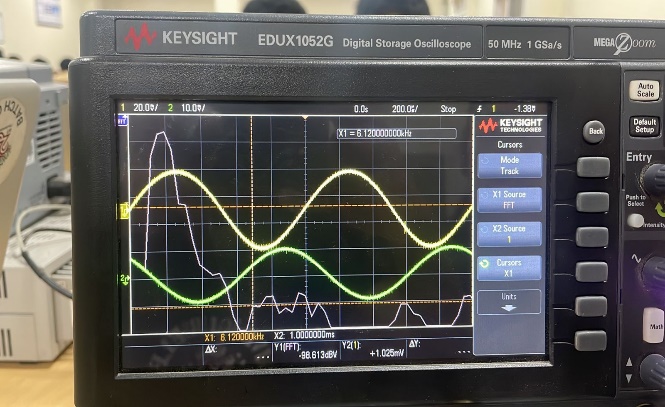
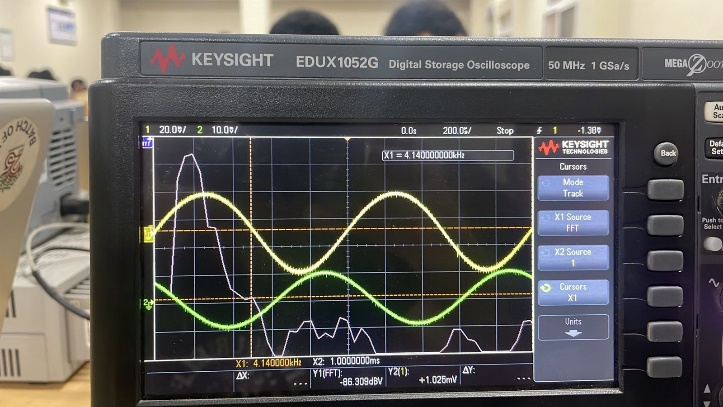
OffSet = -60 dBV

Vin = 2 mV

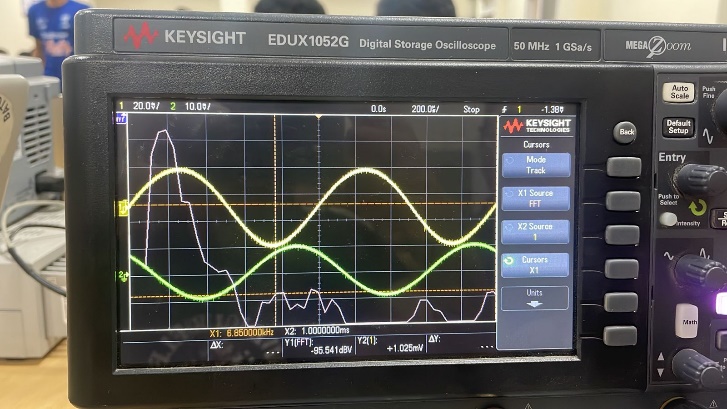
Harmonic 1 Harmonic 2



Harmonic 3 Harmonic 4

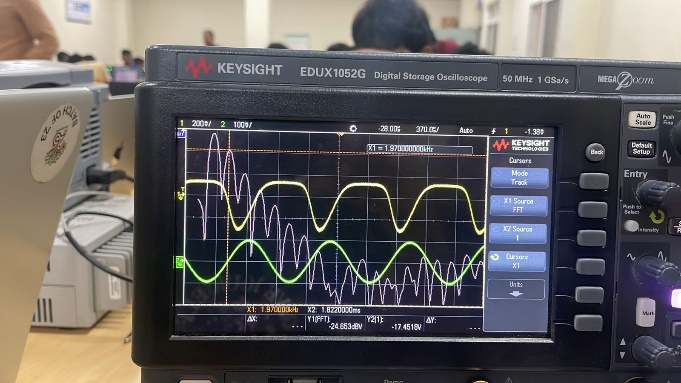


Harmonic 5

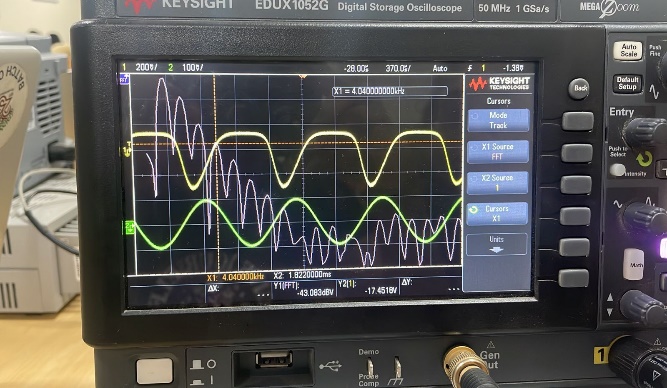
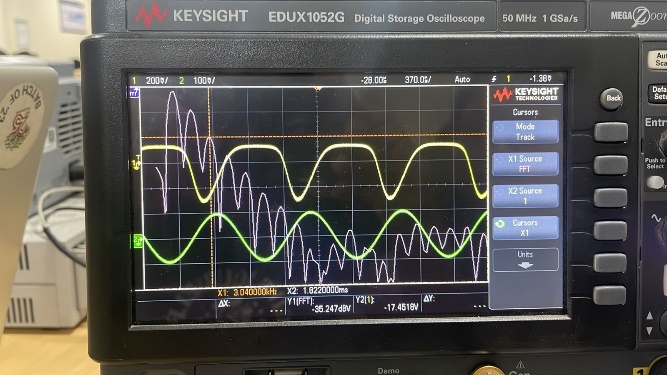


Vin = 100 mV

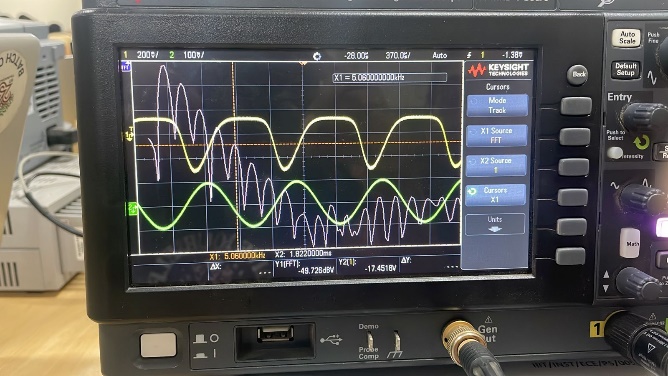
Harmonic 1 Harmonic 2



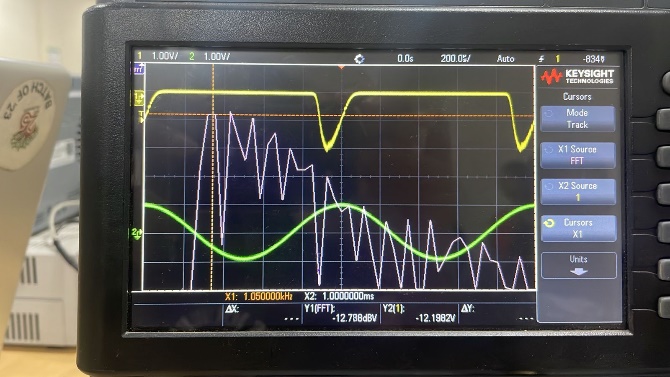
Harmonic 3 Harmonic 4

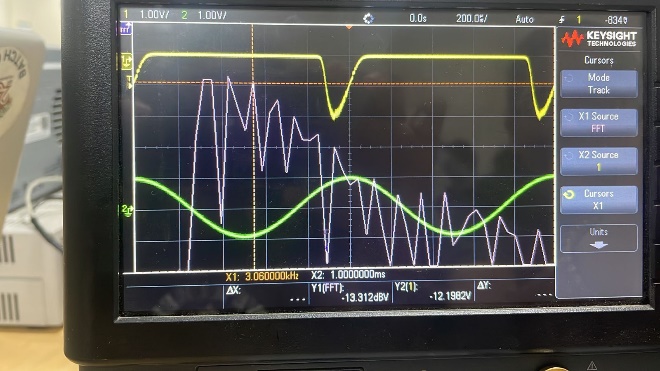


Harmonic 5

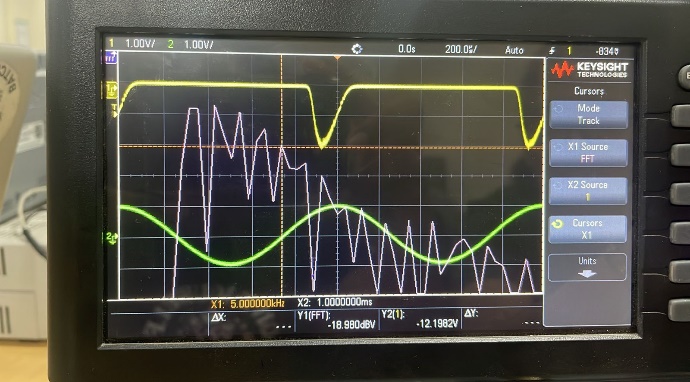
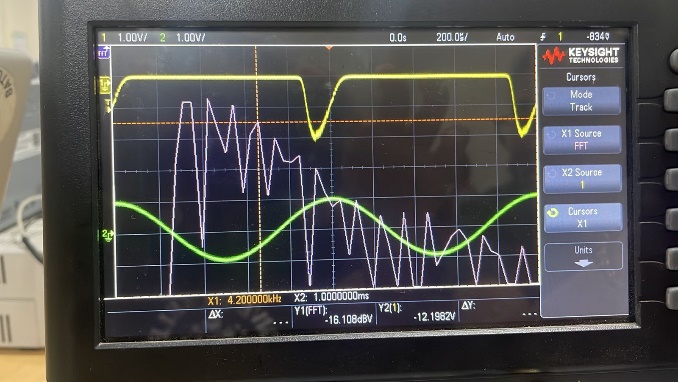


Vin = 2V

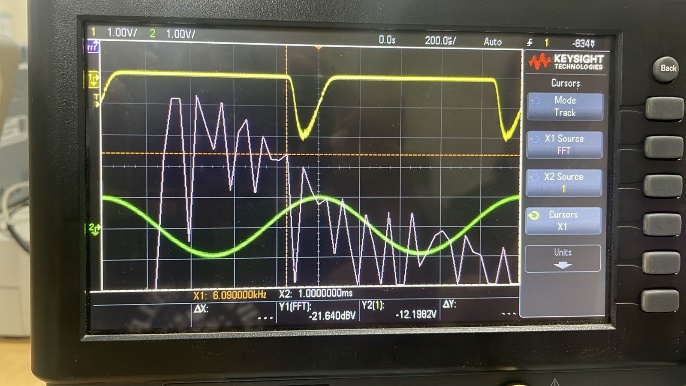
Harmonic 1 Harmonic 2



Harmonic 3 Harmonic 4



Harmonic 5



|  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- |
| **Vin**  **(mV)** | **Vout**  **(mV)** | **Harmonic**  **(V1)(dBV)** | **Harmonic**  **(V1)(dBV)** | **Harmonic**  **(V1)(dBV)** | **Harmonic**  **(V1)(dBV)** | **Harmonic**  **(V1)(dBV)** | **THD**  **(dBV)** | **THD**  **(V)** |
| 2 | 6.85 | -48.90 | -82.98 | -94 | -100.042 | -104.9 | -6.923 | 0.451 |
| 10 | 30.5 | -34.51 | -60.85 | -86.309 | -98.6 | -99.54 | -5.080 | 0.557 |
| 20 | 62.5 | -28.46 | -50.43 | -73.5 | -88.7 | -90.9 | -5.45 | 0.534 |
| 50 | 140 | -21.4 | -34.37 | -49.74 | -61.95 | -78.92 | -5.47 | 0.533 |
| 100 | 230 | -17.4 | -24.6 | -35.2 | -43.0 | -49.7 | -4.86 | 0.571 |
| 500 | 625 | -15.089 | -15.69 | -18.5 | -21.88 | -25.76 | -2.76 | 0.743 |
| 1000 | 1250 | -13.8 | -14.1 | -18.1 | -20.34 | -22.69 | -2.74 | 0.729 |
| 2000 | 2200 | -12.78 | -13.31 | -16.10 | -18.98 | -21.64 | -2.76 | 0.727 |

***3.Frequency Response***

Given,

RL = 1KOhm

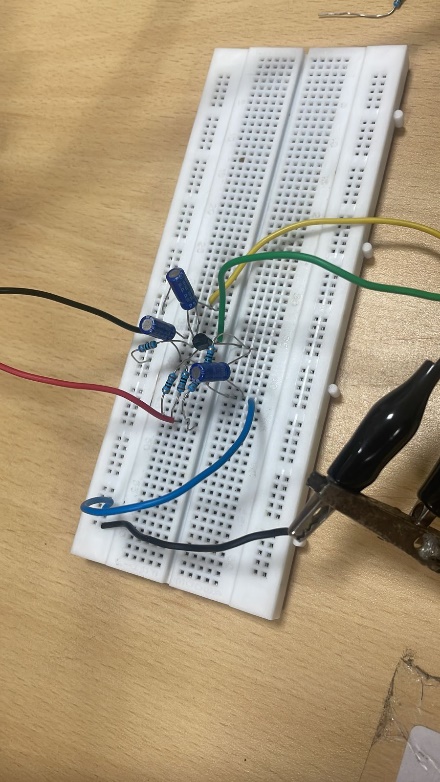
Vin = 10 mV

fin ={10 Hz, 50 Hz, 100 Hz, 500 Hz, 1 kHz, 10 kHz, 100 kHz,1 MHz, 10 MHz, 20 MHz}

To find,

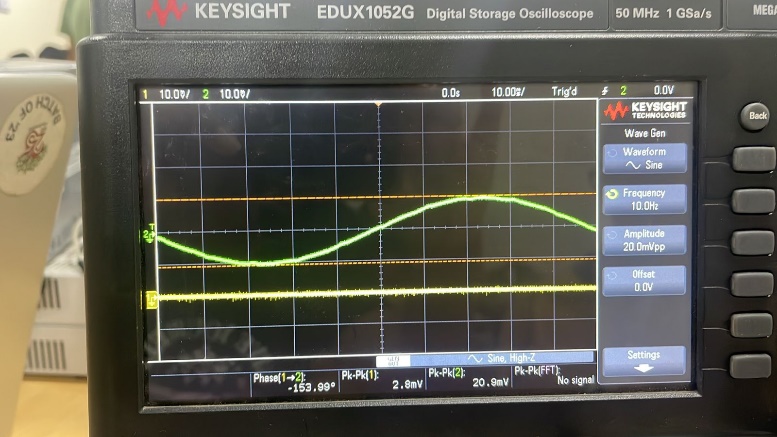
fL (-3dB frequency)

fH (-3dB frequency)

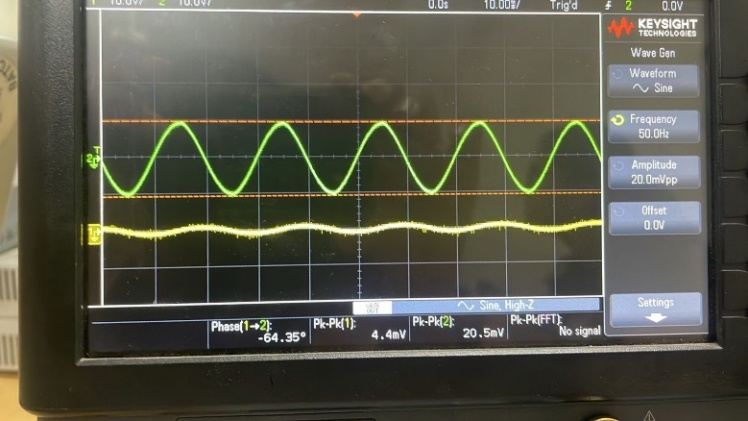


***When LOAD RESISTOR of 1K Ohm is used:***

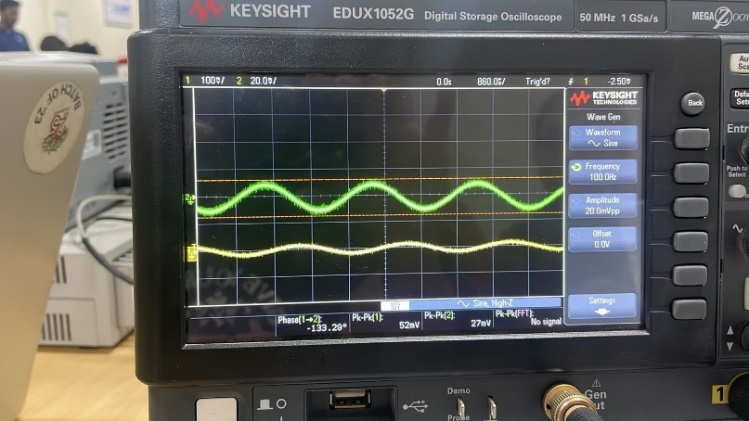
fin = 10Hz



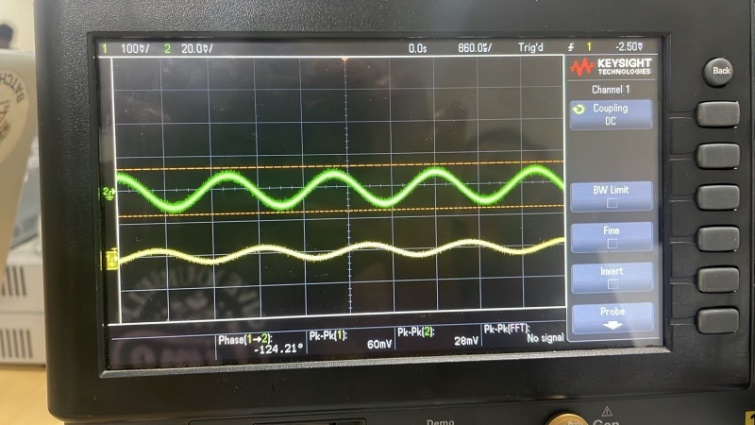
fin = 50Hz

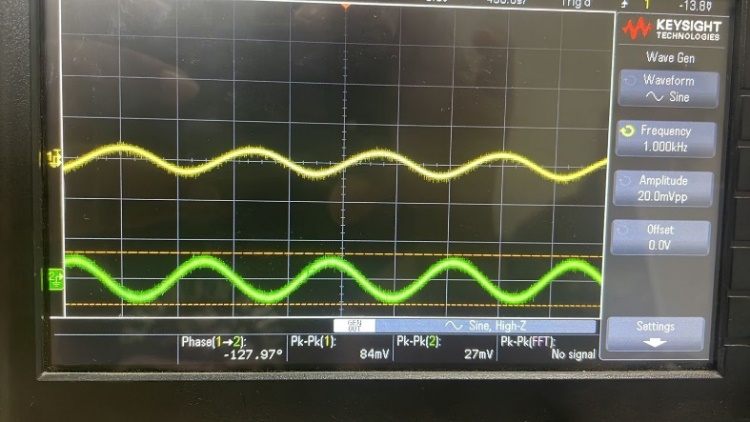


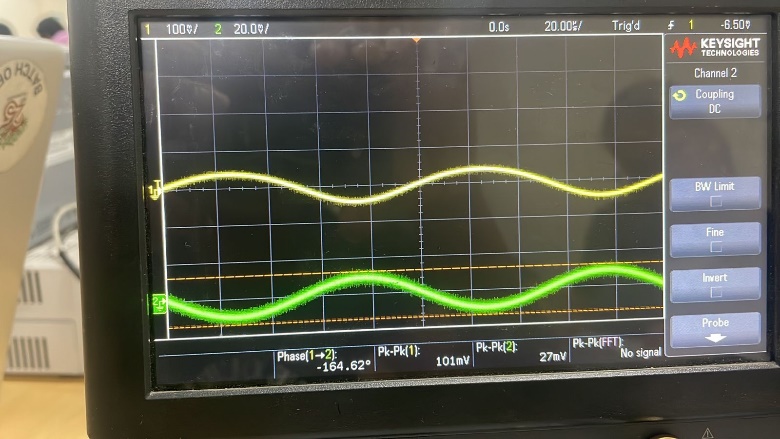
fin = 100Hz



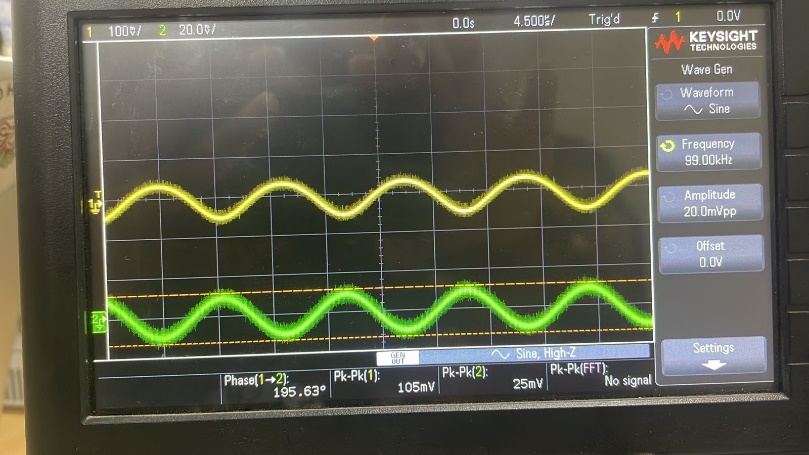
fin = 500Hz



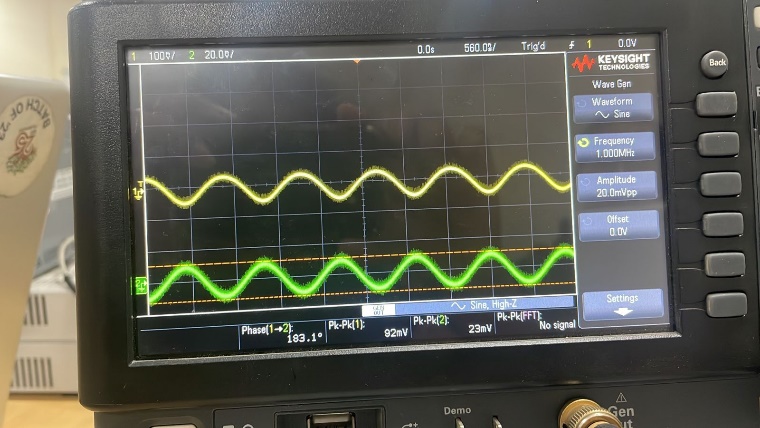
fin = 1k Hz

fin = 10k Hz  


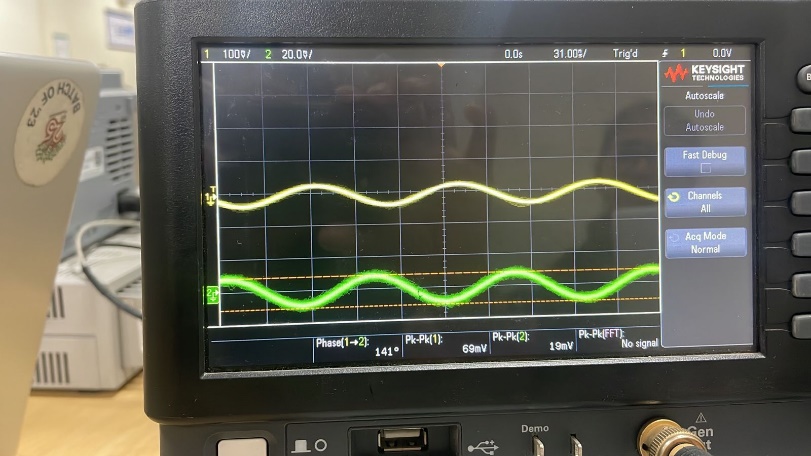
fin = 100kHz



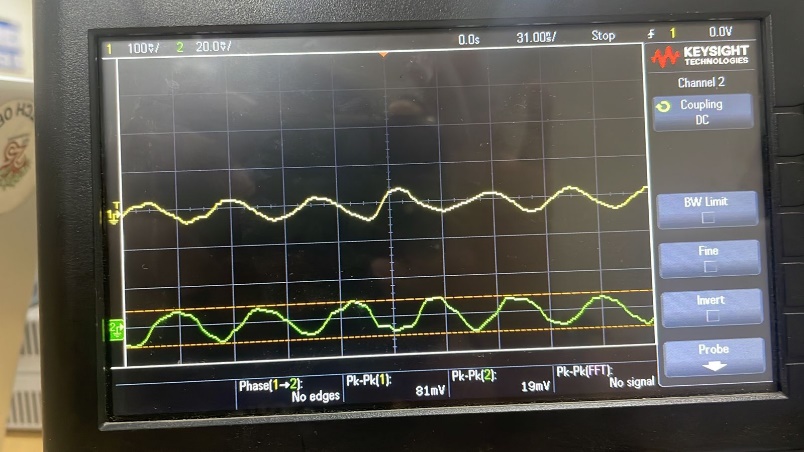
fin = 1MHz



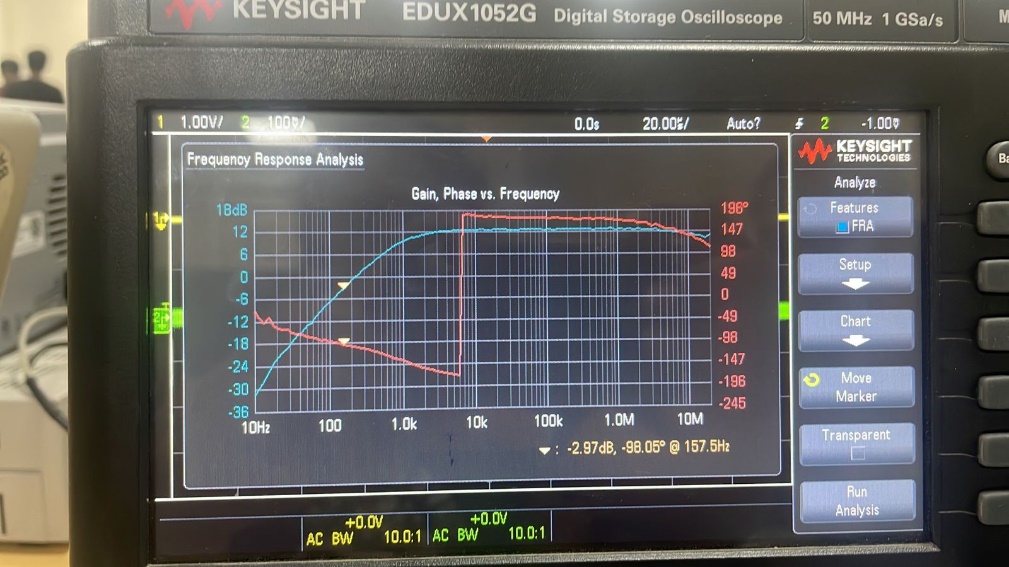
fin = 10MHz



fin = 20MHz



***Frequency Response Analysis:***



**At -3dB frequency, the value of fL = 157.5 Hz**

Because the parasitic capacitance in the circuit is usually relatively low, the -3dB cutoff frequency at higher frequencies is not visible on the graph. The high cutoff frequency resulting from this low capacitance value surpasses the maximum frequency range that the digital storage oscilloscope (DSO) in use can support.

Consequently, the DSO is unable to see or record the high-frequency cutoff region of the graph, when the voltage gain begins to diminish. Due to equipment restrictions, we are unable to observe the circuit's full frequency response, especially at higher frequencies when the low parasitic capacitance causes a high cutoff frequency.

**Calculations:**

* Gain = Av

20 x log(|Av|) = -3

Av = 0.7070

**Hand Calculations for fL and fH:**

* f = 1 / (2πRC)
* Reff = RC || RL = 94.8 || 1k

= 86.59115 ohm

Value of C for fL = 10 uF

Value of C for fH = 15 pF (This is the Parasitic Capacitance that is fixed for a particular BJT)

fL = 1 / (2.π.(10.10-6). 86.59) = 183.89 Hz

fH = 1 / (2.π.15.10-12). 86.59) = 1.225 x 108 Hz

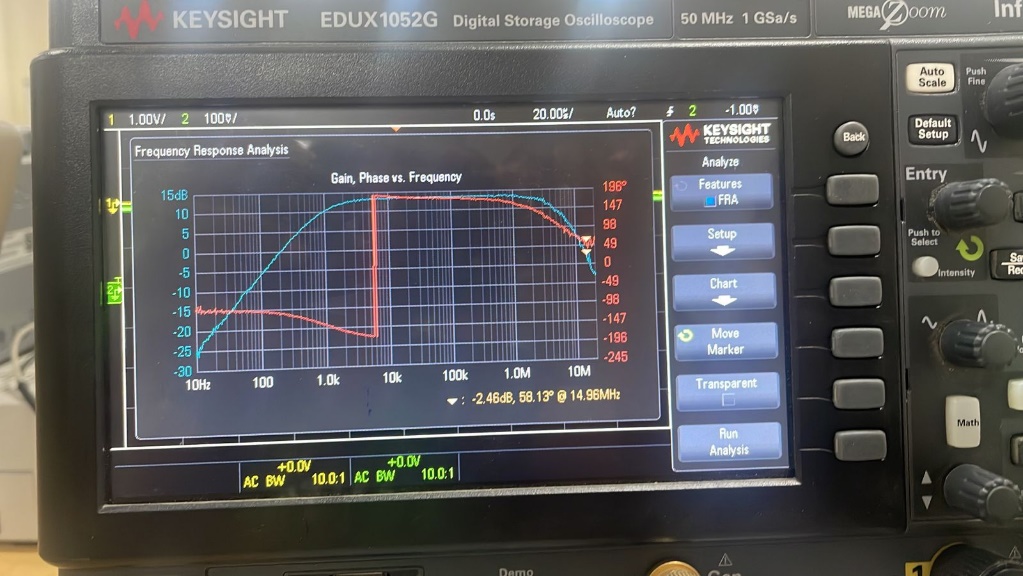
The values of fL and fH obtained from hand calculations

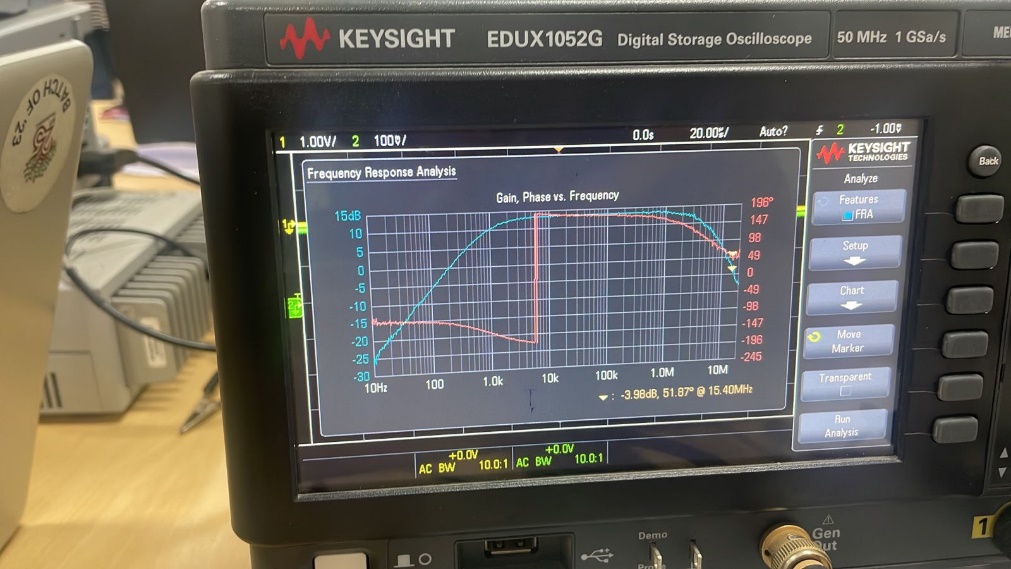
|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| **Input Frequency** | **Vin** | **Vout** | **Voltage Gain(Av)** | **Av(in dB)** |
| 10 Hz | 10.45 | 1.4 | 0.133 | -17.42 |
| 50 Hz | 10.25 | 2 | 0.195 | -14.20 |
| 100 Hz | 10.25 | 26 | 2.53 | 8.66 |
| 500 Hz | 14 | 30 | 2.14 | 6.61 |
| 1k Hz | 13.5 | 42 | 3.11 | 9.86 |
| 10k Hz | 13.5 | 50.5 | 3.74 | 11.46 |
| 100k Hz | 12.5 | 52.5 | 4.2 | 12.46 |
| 1M Hz | 11.5 | 46 | 4 | 12.04 |
| 10M Hz | 9.5 | 32.5 | 3.421 | 12.30 |
| 20M Hz | 9.5 | 31.54 | 3.32 | 12.59 |

***When LOAD CAPACITOR of 440 uF is used:***

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At -3dB frequency, the value of fL = 136.2 Hz





The -3dB frequency of fH is between a range of 14.96 MHz(-2.46 dB) and 15.40 MHz(-3.98 dB)

At -3dB frequency,

**The value of fL = 136.2 Hz**

**The value of fH = 15.2 MHz**

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| **Input Frequency** | **Vin** | **Vout** | **Voltage Gain(Av)** | **Av(in dB)** |
| 10 Hz | 11.5 | 10 | 0.8695 | -1.21 |
| 50 Hz | 10 | 4.82 | 0.482 | -6.34 |
| 100 Hz | 10.25 | 8.16 | 0.7960 | -1.98 |
| 500 Hz | 10.73 | 22.85 | 2.1295 | 6.57 |
| 1k Hz | 10.2 | 34.52 | 3.384 | 10.59 |
| 10k Hz | 9.89 | 51.65 | 5.233 | 14.38 |
| 100k Hz | 9.53 | 52.48 | 5.5068 | 14.82 |
| 1M Hz | 8.1 | 49 | 6.049 | 15.63 |
| 10M Hz | 4.92 | 5.49 | 1.1158 | 0.95 |
| 20M Hz | 1.8 | 0.68 | 0.377 | -8.47 |

**Hand Calculations for fL and fH:**

* f = 1 / (2πRC)
* Reff = RC = 94.8 ohm

Value of C for fL = 10 uF

Value of C for fH = 440 pF (This capacitance is dominant than the parasitic capacitance)

fL = 1 / (2.π.(10.10-6). 94.8) = 167.97 Hz

fH = 1 / (2.π.440.10-12). 94.8) = 3.8 MHz

In this instance, the presence of the capacitor at the load (CL) allows us to observe the cutoff frequency. Because of its functions as a low-pass filter by attenuating higher frequencies and allowing only lower frequencies to pass through.

Through its ability to block or reduce the amplitudes of higher frequencies, the capacitor effectively limits the bandwidth of the circuit. The frequency response graph illustrates this phenomena, which causes the high-frequency components to be cut out. The cutoff frequency and the circuit's overall frequency response are greatly influenced by the presence of the capacitor at the load.

**Reason why a Capacitor is placed in parallel to the resistance at Emitter terminal:**

The capacitor is placed across Re because, in an AC analysis, the presence of RE will reduce the gain. Therefore, we placed a capacitor across Re to raise the gain by acting as a short-circuit in a tiny signal analysis.  
We could have just installed a plane wire in its place, but when we look at the huge signal model, we notice that we need to set the Ve and Vb to zero. Additionally, we need to control through input, so this fixes the Vbe value, which fixes the Ic value, which fixes the Vout. As a result, we are unable to use a plane wire in place of a resistor because doing so would prevent me from receiving the amplified input signal as an output. Because the function generator's highest frequency is lower than the amplifier's upper -3dB frequency, we were unable to determine the fH using the lab's provided equipment.

The presence of the capacitor at the load (CL) in this case makes it possible to observe the cutoff frequency. This is because it functions as a low-pass filter, allowing only lower frequencies to get through while attenuating higher frequencies. The capacitor effectively limits the circuit's bandwidth by attenuating the amplitudes of higher frequencies. This process is illustrated graphically in the frequency response, leading to the elimination of high-frequency components. The presence of the capacitor at the load greatly influences the cutoff frequency and the circuit's overall frequency response.